# A LOW POWER, 3- BIT PIPELINED ADC IN 1.2 V POWER SUPPLY USING CMOS TECHNOLOGY IN MICROWIND SOFTWARE

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## ABSTRACT

*CMOS process technology has been moving rapidly towards finer geomeay for higher system integration faster clock Frequencies and lower power consumption. With deep sub-micron CMOS transistors, voltage supply has been reduced from 5.0V to 3.3V and even to 1.2V. This paper introduces a design that addresses the issues of 1.2V supply in a 3-bit pipeline ADC implemented in a CMOS process. We have Implement here two Different approaches using slight modification .The total power consumption of the Chip approximated half of that reported in first design Approach.*

***Keywords****—CMOS technology, data converter, residue voltage, operational amplifier, power efficiency*

## INTRODUCTION

The current market trend in the semiconductor industry forces the important constraints on the analog circuit designs. First is that the increasing demand for battery operated portable electronic devices including the cellular phones, forces the need to implement Circuits with very low power consumption with not much compromise on the *speed* of operation. Secondly, the reduction of IC supply voltages due to technology **scaling** demands the operation at supply voltages in the range of 1-2V. Finally there is more demand for higher system integration forcing analog designs to be implemented in the digital CMOStechnologies.

Let see how these useful in Pipeline structure.

One circuit type directly affected by this low-voltage problem is the switched-capacitor circuit, used in many practical analog signal processing applications including data converters. The fundamental limitation on the operation of a floating switch arises when the supply voltage becomes less than the sum of the absolute values of the PMOS and NMOS threshold voltages. The best Solution Reported in Pipelined ADC.

**3 stage Pipelined Structure**

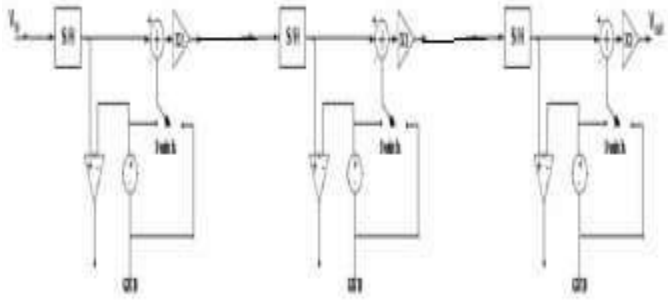

***Fig. 1***

*The structure of each pipeline stage consists of a flash sub- ADC with two comparators and* ***a*** *multiplying-DAC (MDAC) that generates the residue for the following stage,* ***as*** *shown in figure 1The MDAC uses two identical metal capacitors for sampling and amplification for anideal stage gain of 2. The sub-ADC decision points arechosen at +/-(Vref/4), where the ADC input range s from -Vref to +Vref.*

**Algorithm for Pipelined Stage**

If $2V_{in}-V_{ref} > 0$, bit =1, and $V_{residue} = 2V_{in}-V_{ref}$

If $2V_{in}-V_{ref} < 0$, bit =0, and $V_{residue} = 2V_{in}$

Depending on sub-ADC decisions, one of three DAC levels, +Vref, 0, - Vref, is chosen as aninput tothe MDAC. Hence, no modification reference circuit is needed forMDACoperations.

## LOW VOLTAGE ADC DESIGN

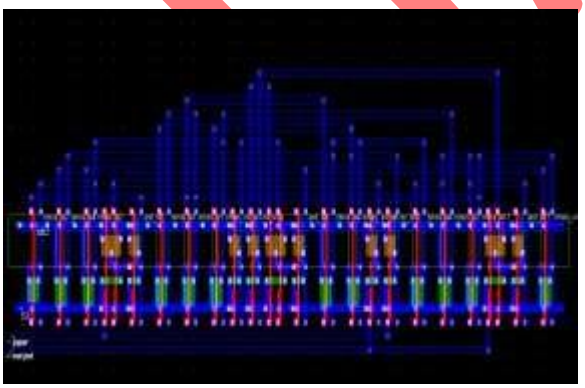

**Fig. 2**

Above Layout is Developed in MicrowindSoftware . It uses 3 pipelined stage CMOStechnology , supply voltage of 1.2 v and frequency approximate 5 GHZ. The circuit Consumed approx. power of 0.50 w by practically shown in below graphs.

## MDAC

As discussed previously a three-stage amplifier was designed to meet the specifications. The first stage uses a telescopic structure with N-channel input transistors. It is followed by a single transistor amplifier stage, as shown in figure 3. The opamp uses two switched capacitor common mode feedback circuitries, one for each stage, which have not been shown in the fig 2. The most critical opamp is the one that is used in the first stage of the pipeline because it has to settle within at least 1- bit accuracy. The two-stage amplifier is compensated by a capacitor with a serial zero-nulling transistor. The biasing circuit was designed to track the variation automatically to size its sensitivity to V variation. Similarly, the telescopic structure tracks input common mode. Simulation showed an output swing > 0.5V and a gain of 1 db with a gain-bandwidth close to 5 GHZ for the opampat1.2V power supply under appropriate loading conditions, discussed later insection.

## SAMPLE AND HOLD

The sample and hold circuit uses a single capacitor switched between input were initial signal and output nodes to signal bandwidth. The operational amplifier used in this circuit has the same architecture as that of the stage amplifiers. Input common mode is provided internally for input signal, therefore, it is not necessary to reject input common mode. The simple architecture allows optimization for fast and linear operation. Placing a sample and hold before stage one allows for the input to stage one in the pipeline to be a discrete time signal which guarantees the MDAC and ADC of stage one operate on the same value if enough time is given to allow the sample-and-hold output to settle to at least 3-bitaccuracy

## OUTPUT VOLTAGES AND CURRENTS

**Fig. 3**

Above fig. 3 shows the output waveforms of the first layout desing as shown in fig. 1. From graph we can conclude that approximate power is 0.50 w Consumed in the design. But much more modification with layout has been done for better outputs below.

**FREQUENCY WAVEFORMS**

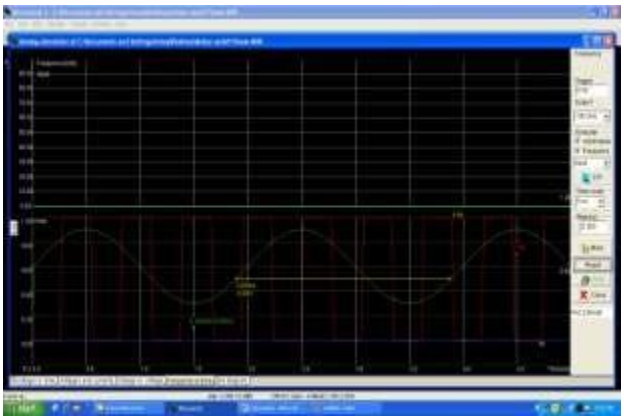

Fig. 4

In this way, both S/H and Gain functions can be implemented within one SC circuit operating much closer to the unity gain frequency of the amplifier. This configuration is often used in the front-end input S/H circuit. It can achieve high speed because the feedback factor can be much larger than that of the previous configuration, operating much closer to the unity gain frequency of the amplifier. For instance, assuming that the closed loop gain is 2 and op amp input capacitance is ignored for simplicity. The important parameters in determining the band width of the SC circuit are Gm (transconductance of the op amp), feedback factor, and output load capacitance. In all of these configurations, the band width is given by,

$$BW = \frac{1}{\tau} = \frac{G_m}{C_{load}} f$$

Where C load is the total capacitance seen at the operational amplifier output. Up to now, discussions presented for the SC configurations are based on the assumption that op amps are ideal. As mentioned previously, the power dissipation in a SC circuit is dominated by the op amp power, and a more realistic op amp must be considered in order to examine its power dissipation and its dependency on other parameters such as technology, supply voltage, etc

## MODIFIED LAYOUT

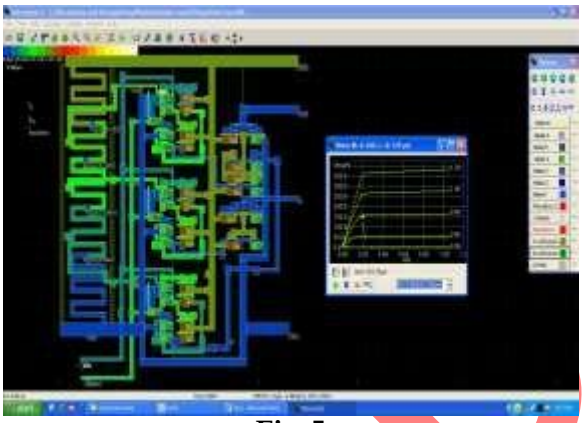

**Fig. 5**

Above fig. 5 show modified layout of the Pipelined ADC in which cascading part now replaced by CMOS technology instead of opamp. So because of that change we find improved performance in power consumption approximately half than last layout.

This function can be implemented using a switched capacitor amplifier as shown in Fig. 5 which uses only two identical capacitors. In the sampling phase, the input is sampled at the bottom plates of capacitors. In the next amplification phase, capacitors are connected in the op-amp feedback paths; the basic operation includes sampling the signal on the sampling capacitor and transferring the signal charge onto the feedback capacitor by using an op amp in the feedback configuration. All charge circuits based on op amps transfer charges between capacitors rather imperfectly because of finite amplifier gain. Consider the multiply by two circuit in Fig 5 with all capacitors matched. In the amplification phase, the summing point moves by –V0/ A0, if the op amp dc gain is finite A. Therefore with 60 and 80-dB op amp gains, the multiply by two output drops by 0.2 and 0.02 percent, respectively. This error can be compensated by using circuit techniques, but the simplest way is to increase dc gain. The signal swing is assumed to be equal to the supply voltage, the maximum voltage swing available in the system. Although the input range of many ADC's is only some fraction of the supply due to a limited op amp output swing, it is a reasonable assumption for the analysis here since the signal swing approximately scales with the supply voltage. At this point, one important design consideration is the choice of Vdsat of the transistor. In real op amps, the output swing and the DC gain requirements set the maximum allowablevoltage.

$$A_v = g_m . R_{out} = \frac{2I_{ds}}{V_{gs} - V_{th}} . \frac{V_A}{I_{ds}} = \frac{2V_A}{V_{dsat}}$$

It can be proven that the settling time of each stage (for linear settling) is given by _sett ln 2,in which _i = RoutiCLiis the time constant of the amplifier. Therefore, according to the model of Fig.5.

$$\tau_{sett} = R_{out_i} C_{L_i} (N - in) \ln 2$$

**V/I GRAPH**

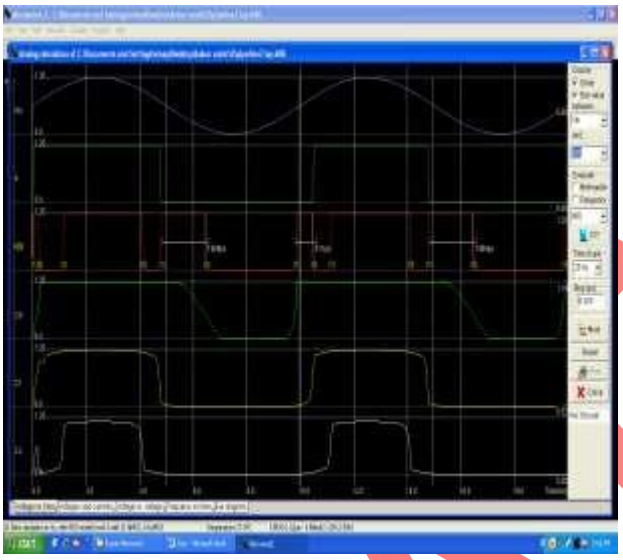

**Fig. 6**

**FREQUENCY RESULTS**

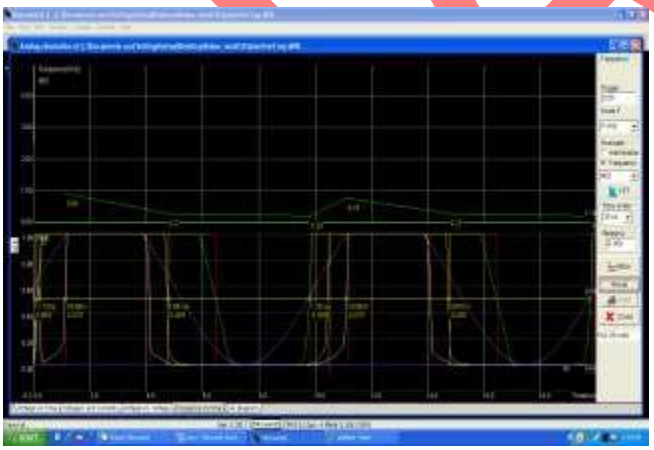

**Fig. 7**

## COMPARISON AND DISCUSSION

To enable a comparison to other ADCs operating at different speeds and resolutions, the figure ofmerit

$$\mathrm{FOM} = \frac{P}{2^{\mathrm{ENOB}} \cdot 2 \cdot f_{\mathrm{in}}}$$

is used , where P is the power consumption, and ENOB is measured for input frequency , not to exceed Nyquist input. It compares state-of-the-art ADCs with sampling rates in excess of 100 MS/s and resolutions of 8 bits or less. From the results, this ADC has one of the best energy efficiencies of published work. In addition, as three out of the four best designs demonstrate, the time-interleaved SAR architecture can achieve very low power for these specifications. This work requires no linearity calibration or digital post-processing of thesamples.

The ADC consumes 2.86 mW and 3.06 mW, respectively, from 1.2-V analog and digital supplies at the maximum sampling frequency. TheADCwas also tested at lower sampling frequencies. At 250 MS/s, the ADC consumes a total of 1.58 mWfrom a 1 V digital and 0.8 V analog supply, while still maintaining Nyquistperformance.

## CONCLUSION

An ADC targeted low Power has been presented. The time-interleaved Pipeline architecture provides superior energy efficiency to a flash converter because of its linear growthin complexity with the resolution. Two new techniques have enabled high-speed, low-power Pipelined operation. The split capacitor array offers both lower switching energy and improved settling speed as compared to the conventional array. Joint timing design of the analog and digital portions of the chip, as demonstrated with the adjustable latch strobing instant, can ease settling time requirements and use otherwise wasted idle time during bit-cycling. State-of-the-art energy efficiency and performance have been demonstrated with robust operation in deep-submicron CMOS.

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